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Stochastic Process Variation in Deep-Submicron CMOS: Circuits and Algorithms (Springer Series in Advanced Microelectronics)

Amir Zjajo

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One of the most notable features of nanometer scale CMOS technology is the increasing magnitude of variability of the key device parameters affecting performance of integrated circuits. The growth of variability can be attributed to multiple factors, including the difficulty of manufacturing control, the emergence of new systematic variation-generating mechanisms, and most importantly, the increase in atomic-scale randomness, where device operation must be described as a *stochastic* process. In addition to *wide-sense stationary stochastic* device variability and temperature variation, existence of *non-stationary stochastic* electrical noise associated with fundamental processes in integrated-circuit devices represents an elementary limit on the performance of electronic circuits.

In an attempt to address these issues, *Stochastic Process Variation in Deep-Submicron CMOS: Circuits and Algorithms* offers unique combination of mathematical treatment of random process variation, electrical noise and temperature and necessary circuit realizations for on-chip monitoring and performance calibration. The associated problems are addressed at various abstraction levels, i.e. circuit level, architecture level and system level. It therefore provides a broad view on the various solutions that have to be used and their possible combination in very effective complementary techniques for both analog/mixed-signal and digital circuits. The feasibility of the described algorithms and built-in circuitry has been verified by measurements from the silicon prototypes fabricated in standard 90 nm and 65 nm CMOS technology.

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