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Logical Effort: Designing Fast CMOS Circuits (The Morgan Kaufmann Series in Computer Architecture and Design)

Ivan Sutherland, Robert F. Sproull, David Harris

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Designers of high-speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets. *Logical Effort: Designing Fast CMOS Circuits* makes high speed design easier and more methodical, providing a simple and broadly applicable method for estimating the delay resulting from factors such as topology, capacitance, and gate sizes.

The brainchild of circuit and computer graphics pioneers Ivan Sutherland and Bob Sproull, "logical effort" will change the way you approach design challenges. This book begins by equipping you with a sound understanding of the method's essential procedures and concepts-so you can start using it immediately. Later chapters explore the theory and finer points of the method and detail its specialized applications.

* Explains the method and how to apply it in two practically focused chapters.
* Improves circuit design intuition by teaching simple ways to discern the consequences of topology and gate size decisions.
* Offers easy ways to choose the fastest circuit from among an array of potential circuit designs.
* Reduces the time spent on tweaking and simulations-so you can rapidly settle on a good design.
* Offers in-depth coverage of specialized areas of application for logical effort: skewed or unbalanced gates, other circuit families (including pseudo-NMOS and domino), wide structures such as decoders, and irregularly forking circuits.
* Presents a complete derivation of the method-so you see how and why it works.

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